



Welcome United States Patent and Trademark Office

☐ Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(((phase and pll and design and simulation and measure)&lt;in&gt;metadata)) &lt;and&gt; (pyr &gt;= 1..."

Your search matched 6 of 1203811 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



## » Search Options

[View Session History](#)[New Search](#)

## Modify Search


☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

## » Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

## Select Article Information

- ☐ 1. **Noise analysis of phase-locked loops**  
 Mehrotra, A.;  
 Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Conference on  
 5-9 Nov. 2000 Page(s):277 - 282  
 Digital Object Identifier 10.1109/ICCAD.2000.896486  
[AbstractPlus](#) | Full Text: [PDF](#)(600 KB) IEEE CNF
- ☐ 2. **A simple method for relating time- and frequency-domain measures of oscillator performance**  
 McNeill, J.A.;  
 Mixed-Signal Design, 2001. SSMSD. 2001 Southwest Symposium on  
 25-27 Feb. 2001 Page(s):7 - 12  
 Digital Object Identifier 10.1109/SSMSD.2001.914928  
[AbstractPlus](#) | Full Text: [PDF](#)(360 KB) IEEE CNF
- ☐ 3. **A dynamically phase adjusting PLL with a variable delay**  
 Yasuda, T.; Fujita, H.; Onodera, H.;  
 Design Automation Conference, 2001. Proceedings of the ASP-DAC 2001. Asia and South Pacific  
 30 Jan.-2 Feb. 2001 Page(s):275 - 280  
 Digital Object Identifier 10.1109/ASPDAC.2001.913318  
[AbstractPlus](#) | Full Text: [PDF](#)(484 KB) IEEE CNF
- ☐ 4. **Substrate coupling analysis and simulation for an industrial phase-locked loop**  
 Welch, R.J.; Yang, A.T.;  
 Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on  
 Volume 6, 31 May-3 June 1998 Page(s):94 - 97 vol.6  
 Digital Object Identifier 10.1109/ISCAS.1998.705220  
[AbstractPlus](#) | Full Text: [PDF](#)(432 KB) IEEE CNF
- ☐ 5. **Differential CMOS circuits for 622-MHz/933-MHz clock and data recovery applications**  
 Djahanshahi, H.; Salama, C.A.T.;  
 Solid-State Circuits, IEEE Journal of  
 Volume 35, Issue 6, June 2000 Page(s):847 - 855  
 Digital Object Identifier 10.1109/4.845188  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(592 KB) IEEE JNL
- ☐ 6. **Analog and mixed-signal benchmark circuits-first release**  
 Kaminska, B.; Arabi, K.; Bell, I.; Goteti, P.; Huertas, J.L.; Kim, B.; Rueda, A.; Soma, M.;

Test Conference, 1997. Proceedings., International  
1-6 Nov. 1997 Page(s):183 - 190  
Digital Object Identifier 10.1109/TEST.1997.639612  
[AbstractPlus](#) | Full Text: [PDF](#)(644 KB) IEEE CNF



Indexed by  
 Inspec

[Help](#) [Contact Us](#) [Privac](#)  
© Copyright 2005 IE

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#)

Welcome United States Patent and Trademark Office

☐ Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(((phase and pll and chip and spice and jitter)&lt;in&gt;metadata)) &lt;and&gt; (pyr &gt;= 1990 &lt;...)"

[e-mail](#)

Your search matched 1 of 1203811 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

## » Search Options

[View Session History](#)[New Search](#)

## Modify Search

 ☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

## » Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard



## 1. A simple precharged CMOS phase frequency detector

Johansson, H.O.;

Solid-State Circuits, IEEE Journal of

Volume 33, Issue 2, Feb. 1998 Page(s):295 - 299

Digital Object Identifier 10.1109/4.658634

[AbstractPlus](#) | [References](#) | Full Text: PDF(124 KB) IEEE JNLIndexed by  
[Help](#) [Contact Us](#) [Privacy](#)

© Copyright 2005 IE



Welcome United States Patent and Trademark Office

☐ Search Results

[BROWSE](#)
[SEARCH](#)
[IEEE XPLORE GUIDE](#)

Results for "(((phase and pll and jitter and test)&lt;in&gt;metadata)) &lt;and&gt; (pyr &gt;= 1990 &lt;and&gt; pyr &lt;= 2000)"

Your search matched 34 of 1203811 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

e-mail

## » Search Options

[View Session History](#)
[New Search](#)

## Modify Search


☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

## » Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

☐ Select Article Information

- ☐ 1. **Low-cost jitter measurement technique for phase-locked loops**  
 Voorakaranam, R.; Chatterjee, A.;  
 Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on  
 Volume 2, 8-11 Aug. 2000 Page(s):956 - 959 vol.2  
 Digital Object Identifier 10.1109/MWSCAS.2000.952912  
[AbstractPlus](#) | Full Text: [PDF](#)(296 KB) IEEE CNF
- ☐ 2. **BIST for phase-locked loops in digital applications**  
 Sunter, S.; Roy, A.;  
 Test Conference, 1999. Proceedings. International  
 28-30 Sept. 1999 Page(s):532 - 540  
 Digital Object Identifier 10.1109/TEST.1999.805777  
[AbstractPlus](#) | Full Text: [PDF](#)(716 KB) IEEE CNF
- ☐ 3. **Stimulus generation for built-in self-test of charge-pump phase-locked loops**  
 Veillette, B.R.; Roberts, G.W.;  
 Test Conference, 1998. Proceedings. International  
 18-23 Oct. 1998 Page(s):698 - 707  
 Digital Object Identifier 10.1109/TEST.1998.743214  
[AbstractPlus](#) | Full Text: [PDF](#)(732 KB) IEEE CNF
- ☐ 4. **On-chip measurement of the jitter transfer function of charge-pump phase-locked loops**  
 Veillette, B.R.; Roberts, G.W.;  
 Test Conference, 1997. Proceedings., International  
 1-6 Nov. 1997 Page(s):776 - 785  
 Digital Object Identifier 10.1109/TEST.1997.639691  
[AbstractPlus](#) | Full Text: [PDF](#)(788 KB) IEEE CNF
- ☐ 5. **Full CMOS video line-locked phase-locked loop system**  
 Rodda, W.E.; Campbell, E.R.; Sauer, D.J.; Mayweather, W.T.; Dell'ova, F.;  
 Consumer Electronics, IEEE Transactions on  
 Volume 39, Issue 3, Aug. 1993 Page(s):496 - 503  
 Digital Object Identifier 10.1109/30.234626  
[AbstractPlus](#) | Full Text: [PDF](#)(548 KB) IEEE JNL
- ☐ 6. **On-chip measurement of the jitter transfer function of charge-pump phase-locked loops**  
 Veillette, B.R.; Roberts, G.W.;

Solid-State Circuits, IEEE Journal of  
Volume 33, Issue 3, March 1998 Page(s):483 - 491  
Digital Object Identifier 10.1109/4.661214

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(192 KB\)](#) IEEE JNL



**7. Measuring jitter and phase error in microprocessor phase-locked loops**

Jenkins, K.A.; Eckhardt, J.P.;  
Design & Test of Computers, IEEE  
Volume 17, Issue 2, April-June 2000 Page(s):86 - 93  
Digital Object Identifier 10.1109/54.844337

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(116 KB\)](#) IEEE JNL



**8. Jitter in ring oscillators**

McNeill, J.A.;  
Solid-State Circuits, IEEE Journal of  
Volume 32, Issue 6, June 1997 Page(s):870 - 879  
Digital Object Identifier 10.1109/4.585289

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(276 KB\)](#) IEEE JNL



**9. A simple precharged CMOS phase frequency detector**

Johansson, H.O.;  
Solid-State Circuits, IEEE Journal of  
Volume 33, Issue 2, Feb. 1998 Page(s):295 - 299  
Digital Object Identifier 10.1109/4.658634

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(124 KB\)](#) IEEE JNL



**10. Verification of embedded phase-locked loops**

Egan, T.; Mourad, S.;  
Quality Electronic Design, 2001 International Symposium on  
26-28 March 2001 Page(s):290 - 295  
Digital Object Identifier 10.1109/ISQED.2001.915245

[AbstractPlus](#) | Full Text: [PDF\(685 KB\)](#) IEEE CNF



**11. Jitter minimization technique for mixed signal testing**

Furukawa, Y.; Kimura, M.; Sugai, M.; Kimura, S.; Purtell, M.;  
Test Conference, 1990. Proceedings., International  
10-14 Sept. 1990 Page(s):613 - 619  
Digital Object Identifier 10.1109/TEST.1990.114075

[AbstractPlus](#) | Full Text: [PDF\(300 KB\)](#) IEEE CNF



**12. Sub-picosecond jitter SiGe BICMOS transmit and receive PLLs for 12.5 Gbaud serial data co**

Friedman, D.; Meghelli, M.; Parker, B.; Ainspan, H.; Soyuer, M.;  
VLSI Circuits, 2000. Digest of Technical Papers. 2000 Symposium on  
15-17 June 2000 Page(s):132 - 135  
Digital Object Identifier 10.1109/VLSIC.2000.852870

[AbstractPlus](#) | Full Text: [PDF\(448 KB\)](#) IEEE CNF



**13. SiGe clock and data recovery IC with linear-type PLL for 10-Gb/s SONET application**

Greshishchev, Y.M.; Schvan, P.;  
Solid-State Circuits, IEEE Journal of  
Volume 35, Issue 9, Sept. 2000 Page(s):1353 - 1359  
Digital Object Identifier 10.1109/4.868047

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(512 KB\)](#) IEEE JNL



**14. A method for measuring the cycle-to-cycle period jitter of high-frequency clock signals**

Yamaguchi, T.J.; Soma, M.; Halter, D.; Raina, R.; Nissen, J.; Ishida, M.;  
VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001  
29 April-3 May 2001 Page(s):102 - 110

Digital Object Identifier 10.1109/VTs.2001.923425

[AbstractPlus](#) | Full Text: [PDF](#)(612 KB) IEEE CNF

- ☐ 15. **A noise-immune GHz-clock distribution scheme using synchronous distributed oscillators**  
Mizuno, H.; Ishibashi, K.;  
Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE Interna  
5-7 Feb. 1998 Page(s):404 - 405, 474  
Digital Object Identifier 10.1109/ISSCC.1998.672558  
[AbstractPlus](#) | Full Text: [PDF](#)(892 KB) IEEE CNF
  
- ☐ 16. **General SSCr vs. cycle-to-cycle jitter relationship with application to the phase noise in PLI**  
Zanchi, A.; Bonfanti, A.; Levantino, S.; Samori, C.;  
Mixed-Signal Design, 2001. SSMSD. 2001 Southwest Symposium on  
25-27 Feb. 2001 Page(s):32 - 37  
Digital Object Identifier 10.1109/SSMSD.2001.914933  
[AbstractPlus](#) | Full Text: [PDF](#)(448 KB) IEEE CNF
  
- ☐ 17. **A new approach for computation of timing jitter in phase locked loops**  
Gourary, M.M.; Rusakov, S.G.; Ulyanov, S.L.; Zharov, M.M.; Gullapalli, K.K.; Mulvaney, B.J.;  
Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings  
27-30 March 2000 Page(s):345 - 349  
Digital Object Identifier 10.1109/DATE.2000.840294  
[AbstractPlus](#) | Full Text: [PDF](#)(44 KB) IEEE CNF
  
- ☐ 18. **Extraction of peak-to-peak and RMS sinusoidal jitter using an analytic signal method**  
Yamaguchi, T.J.; Soma, M.; Ishida, M.; Watanabe, T.; Ohmi, T.;  
VLSI Test Symposium, 2000. Proceedings. 18th IEEE  
30 April-4 May 2000 Page(s):395 - 402  
Digital Object Identifier 10.1109/VTEST.2000.843870  
[AbstractPlus](#) | Full Text: [PDF](#)(316 KB) IEEE CNF
  
- ☐ 19. **Characterization and verification of phase-locked loops**  
Egan, T.; Mourad, S.;  
Instrumentation and Measurement Technology Conference, 2001. IMTC 2001. Proceedings of the  
Volume 3, 21-23 May 2001 Page(s):1697 - 1702 vol.3  
Digital Object Identifier 10.1109/IMTC.2001.929491  
[AbstractPlus](#) | Full Text: [PDF](#)(588 KB) IEEE CNF
  
- ☐ 20. **The effect of period generation techniques on period resolution and waveform jitter in VLSI**  
Davis, M.G.;  
Test Conference, 1996. Proceedings., International  
20-25 Oct. 1996 Page(s):685 - 690  
Digital Object Identifier 10.1109/TEST.1996.557126  
[AbstractPlus](#) | Full Text: [PDF](#)(456 KB) IEEE CNF
  
- ☐ 21. **Jitter measurements of a PowerPC<sup>TM</sup> microprocessor using an analytic signal method**  
Yamaguchi, T.J.; Soma, M.; Halter, D.; Nissen, J.; Raina, R.; Ishida, M.; Watanabe, T.;  
Test Conference, 2000. Proceedings. International  
3-5 Oct. 2000 Page(s):955 - 964  
Digital Object Identifier 10.1109/TEST.2000.894307  
[AbstractPlus](#) | Full Text: [PDF](#)(704 KB) IEEE CNF
  
- ☐ 22. **Achieving  $\pm 30$  ps accuracy in the ATE environment**  
Petrich, D.;  
Test Conference, 1994. Proceedings., International  
2-6 Oct. 1994 Page(s):691 - 700  
Digital Object Identifier 10.1109/TEST.1994.528015

[AbstractPlus](#) | Full Text: [PDF](#)(580 KB) IEEE CNF

- ☐ **23. A monolithic 156 Mb/s clock and data recovery PLL circuit using the sample-and-hold techn**  
Ishihara, N.; Akazawa, Y.;  
Solid-State Circuits, IEEE Journal of  
Volume 29, Issue 12, Dec. 1994 Page(s):1566 - 1571  
Digital Object Identifier 10.1109/4.340432

[AbstractPlus](#) | Full Text: [PDF](#)(512 KB) IEEE JNL

- ☐ **24. Differential CMOS circuits for 622-MHz/933-MHz clock and data recovery applications**  
Djahanshahi, H.; Salama, C.A.T.;  
Solid-State Circuits, IEEE Journal of  
Volume 35, Issue 6, June 2000 Page(s):847 - 855  
Digital Object Identifier 10.1109/4.845188

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(592 KB) IEEE JNL

- ☐ **25. A monolithic 2.3-Gb/s 100-mW clock and data recovery circuit in silicon bipolar technology**  
Soyuer, M.;  
Solid-State Circuits, IEEE Journal of  
Volume 28, Issue 12, Dec. 1993 Page(s):1310 - 1313  
Digital Object Identifier 10.1109/4.262004

[AbstractPlus](#) | Full Text: [PDF](#)(400 KB) IEEE JNL



Indexed by  
 Inspec

[Help](#) [Contact Us](#) [Privac](#)

© Copyright 2005 IE



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(((phase and pll and simulate)&lt;in&gt;metadata)) &lt;and&gt; (pyr &gt;= 1990 &lt;and&gt; pyr &lt;= ..."

Your search matched 44 of 1203811 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



## » Search Options

[View Session History](#)
[New Search](#)

## Modify Search


☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

## » Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

## Select Article Information

- ☐ 1. **NDA PLL design for carrier phase recovery of QPSK/TDMA bursts without preamble**  
 Junghoon Lee;  
 Statistical Signal and Array Processing, 2000. Proceedings of the Tenth IEEE Workshop on  
 14-16 Aug. 2000 Page(s):660 - 663  
 Digital Object Identifier 10.1109/SSAP.2000.870208  
[AbstractPlus](#) | Full Text: [PDF](#)(252 KB) IEEE CNF
- ☐ 2. **Designing on-chip clock generators**  
 Chen, D.-L.;  
 Circuits and Devices Magazine, IEEE  
 Volume 8, Issue 4, July 1992 Page(s):32 - 36  
 Digital Object Identifier 10.1109/101.146301  
[AbstractPlus](#) | Full Text: [PDF](#)(448 KB) IEEE JNL
- ☐ 3. **Cycle-domain simulator for phase-locked loops**  
 James, N.K.;  
 Mixed-Signal Design, 2000. SSMSD. 2000 Southwest Symposium on  
 27-29 Feb. 2000 Page(s):77 - 82  
 Digital Object Identifier 10.1109/SSMSD.2000.836450  
[AbstractPlus](#) | Full Text: [PDF](#)(196 KB) IEEE CNF
- ☐ 4. **CMOS wide-swing differential VCO for fully integrated fast PLL**  
 Fouzar, Y.; Sawan, M.; Savaria, Y.;  
 Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on  
 Volume 2, 8-11 Aug. 2000 Page(s):948 - 950 vol.2  
 Digital Object Identifier 10.1109/MWSCAS.2000.952910  
[AbstractPlus](#) | Full Text: [PDF](#)(192 KB) IEEE CNF
- ☐ 5. **Optical homodyne receiver based on an improved balance phase-locked loop with the data-crosstalk suppression**  
 Sun, L.; Ye, P.;  
 Photonics Technology Letters, IEEE  
 Volume 2, Issue 9, Sept. 1990 Page(s):678 - 679  
 Digital Object Identifier 10.1109/68.59348  
[AbstractPlus](#) | Full Text: [PDF](#)(144 KB) IEEE JNL
- ☐ 6. **Very short locking time PLL based on controlled gain technique**

Fouzar, Y.; Sawan, M.; Savaria, Y.;  
Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on  
Volume 1, 17-20 Dec. 2000 Page(s):252 - 255 vol.1  
Digital Object Identifier 10.1109/ICECS.2000.911531  
[AbstractPlus](#) | Full Text: [PDF](#)(256 KB) IEEE CNF

- ☐ 7. **A differential type CMOS phase frequency detector**  
Chang, R.C.; Lung-Chih Kuo;  
ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on  
28-30 Aug. 2000 Page(s):61 - 64  
Digital Object Identifier 10.1109/APASIC.2000.896908  
[AbstractPlus](#) | Full Text: [PDF](#)(264 KB) IEEE CNF
  
- ☐ 8. **Characterization, simulation and modeling of PLL under irradiation using HDL-A**  
Martinez, I.; Delatte, P.; Flandre, D.;  
Behavioral Modeling and Simulation, 2000. Proceedings. 2000 IEEE/ACM International Workshop  
19-20 Oct. 2000 Page(s):57 - 61  
Digital Object Identifier 10.1109/BMAS.2000.888365  
[AbstractPlus](#) | Full Text: [PDF](#)(272 KB) IEEE CNF
  
- ☐ 9. **Digital frequency synthesizer/modulator for continuous-phase modulations with slow frequency**  
Vankka, J.;  
Vehicular Technology, IEEE Transactions on  
Volume 46, Issue 4, Nov. 1997 Page(s):933 - 940  
Digital Object Identifier 10.1109/25.653067  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(184 KB) IEEE JNL
  
- ☐ 10. **Applications of an envelope simulator**  
Howard, A.;  
ARFTG Conference Digest, 1998. Computer-Aided Design and Test for High-Speed Electronics. 5;  
3-4 Dec. 1998 Page(s):39 - 54  
Digital Object Identifier 10.1109/ARFTG.1998.768623  
[AbstractPlus](#) | Full Text: [PDF](#)(956 KB) IEEE CNF
  
- ☐ 11. **Performance of phase-locked loop receiver in digital FM systems**  
Ekvetchavit, T.; Zvonar, Z.;  
Personal, Indoor and Mobile Radio Communications, 1998. The Ninth IEEE International Symposium  
Volume 1, 8-11 Sept. 1998 Page(s):381 - 385 vol.1  
Digital Object Identifier 10.1109/PIMRC.1998.733583  
[AbstractPlus](#) | Full Text: [PDF](#)(432 KB) IEEE CNF
  
- ☐ 12. **A simple method for relating time- and frequency-domain measures of oscillator performance**  
McNeill, J.A.;  
Mixed-Signal Design, 2001. SSMSD. 2001 Southwest Symposium on  
25-27 Feb. 2001 Page(s):7 - 12  
Digital Object Identifier 10.1109/SSMSD.2001.914928  
[AbstractPlus](#) | Full Text: [PDF](#)(360 KB) IEEE CNF
  
- ☐ 13. **Mixed-mode simulation of phase-locked loops**  
Antao, B.A.A.; El-Turky, F.M.; Leonowich, R.H.;  
Custom Integrated Circuits Conference, 1993., Proceedings of the IEEE 1993  
9-12 May 1993 Page(s):8.4.1 - 8.4.4  
Digital Object Identifier 10.1109/CICC.1993.590585  
[AbstractPlus](#) | Full Text: [PDF](#)(328 KB) IEEE CNF
  
- ☐ 14. **A 3 V 200 MHz PLL with a low-noise VCO based on a power-efficient low-ripple DC-DC converter**  
Seung-Chul Lee; Joon-Seok Lee; Sung-Ho Lee; Seung-Hoon Lee;  
VLSI and CAD, 1999. ICVC '99. 6th International Conference on

26-27 Oct. 1999 Page(s):346 - 348  
Digital Object Identifier 10.1109/CVC.1999.820928  
[AbstractPlus](#) | Full Text: [PDF](#)(180 KB) IEEE CNF

- ☐ **15. A VCO jitter performance comparison of frequency synthesizer with analog-HDL and SPICE**  
Min-Ho Kim; Jong-Wha Chong;  
TENCON 99. Proceedings of the IEEE Region 10 Conference  
Volume 2, 15-17 Sept. 1999 Page(s):1034 - 1037 vol.2  
Digital Object Identifier 10.1109/TENCON.1999.818598  
[AbstractPlus](#) | Full Text: [PDF](#)(184 KB) IEEE CNF
  
- ☐ **16. Digital frequency synthesizer/modulator for continuous phase modulations with slow frequency**  
Vankka, J.;  
Personal, Indoor and Mobile Radio Communications, 1996. PIMRC'96., Seventh IEEE International  
Volume 3, 15-18 Oct. 1996 Page(s):1039 - 1043 vol.3  
Digital Object Identifier 10.1109/PIMRC.1996.568440  
[AbstractPlus](#) | Full Text: [PDF](#)(548 KB) IEEE CNF
  
- ☐ **17. An integrated PLL clock generator for 275 MHz graphic displays**  
Gutierrez, G.; DeSimone, D.;  
Custom Integrated Circuits Conference, 1990., Proceedings of the IEEE 1990  
13-16 May 1990 Page(s):15.1/1 - 15.1/4  
Digital Object Identifier 10.1109/CICC.1990.124742  
[AbstractPlus](#) | Full Text: [PDF](#)(344 KB) IEEE CNF
  
- ☐ **18. PLL FM demodulator performance under Gaussian modulation**  
Hasan, P.;  
Communications, IEEE Transactions on  
Volume 46, Issue 4, April 1998 Page(s):437 - 440  
Digital Object Identifier 10.1109/26.664295  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(128 KB) IEEE JNL
  
- ☐ **19. VCO jitter simulation and its comparison with measurement**  
Takahashi, M.; Ogawa, K.; Kundert, K.S.;  
Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia and South Pacific  
18-21 Jan. 1999 Page(s):85 - 88 vol.1  
Digital Object Identifier 10.1109/ASPDAC.1999.759717  
[AbstractPlus](#) | Full Text: [PDF](#)(324 KB) IEEE CNF
  
- ☐ **20. Behavioral modeling of a phase locked loop**  
Phanse, A.; Shirani, R.; Rasmussen, R.; Mendel, R.; Yuan, J.S.;  
Southcon/96. Conference Record  
25-27 June 1996 Page(s):400 - 404  
Digital Object Identifier 10.1109/SOUTHCON.1996.535101  
[AbstractPlus](#) | Full Text: [PDF](#)(340 KB) IEEE CNF
  
- ☐ **21. Estimating and interpreting the instantaneous frequency of a signal. II. Algorithms and applications**  
Boashash, B.;  
Proceedings of the IEEE  
Volume 80, Issue 4, April 1992 Page(s):540 - 568  
Digital Object Identifier 10.1109/5.135378  
[AbstractPlus](#) | Full Text: [PDF](#)(1956 KB) IEEE JNL
  
- ☐ **22. All-digital reverse modulation architecture based carrier recovery implementation for GMSK FQPSK**  
Wei Gao; Feher, K.;  
Broadcasting, IEEE Transactions on  
Volume 42, Issue 1, March 1996 Page(s):55 - 62

Digital Object Identifier 10.1109/11.486076

[AbstractPlus](#) | Full Text: [PDF](#)(912 KB) IEEE JNL



**23. A current-controlled oscillator coarse-steering acquisition-aid for high frequency SOI CMOS**

Yi-Chang; Greeneich, E.W.;

Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on  
Volume 2, 30 May-2 June 1999 Page(s):561 - 564 vol.2

Digital Object Identifier 10.1109/ISCAS.1999.780814

[AbstractPlus](#) | Full Text: [PDF](#)(280 KB) IEEE CNF



**24. Design of low jitter PLL for clock generator with supply noise insensitive VCO**

Chang-Hyeon Lee; Cornish, J.; McClellan, K.; Choma, J., Jr.;

Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on  
Volume 1, 31 May-3 June 1998 Page(s):233 - 236 vol.1

Digital Object Identifier 10.1109/ISCAS.1998.704272

[AbstractPlus](#) | Full Text: [PDF](#)(400 KB) IEEE CNF



**25. Reducing the PLL noise bandwidth by a digital split-loop**

Gustrau, J.; Hoffmann, M.H.;

Communications Letters, IEEE

Volume 3, Issue 4, April 1999 Page(s):111 - 112

Digital Object Identifier 10.1109/4234.757205

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(44 KB) IEEE JNL



Indexed by  
 Inspec

[Help](#) [Contact Us](#) [Privacy](#)

© Copyright 2005 IE



Welcome United States Patent and Trademark Office

☐ Search Results

## BROWSE

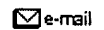
## SEARCH

## IEEE XPLORE GUIDE

Results for "(((phase and pll and simulate and jitter)&lt;in&gt;metadata)) &lt;and&gt; (pyr &gt;= 1990 &lt;and&gt;..."

Your search matched 13 of 1203811 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



## » Search Options

[View Session History](#)[New Search](#)

## Modify Search


☐ Check to search only within this results set

 Display Format: ☒ Citation ☐ Citation & Abstract

## » Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

## Select Article Information

- |                          |  |
|--------------------------|--|
| <input type="checkbox"/> | <p><b>1. A VCO jitter performance comparison of frequency synthesizer with analog-HDL and SPICE</b><br/>         Min-Ho Kim; Jong-Wha Chong;<br/>         TENCON 99. Proceedings of the IEEE Region 10 Conference<br/>         Volume 2, 15-17 Sept. 1999 Page(s):1034 - 1037 vol.2<br/>         Digital Object Identifier 10.1109/TENCON.1999.818598<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF</a>(184 KB) IEEE CNF</p>  |
| <input type="checkbox"/> | <p><b>2. A simple method for relating time- and frequency-domain measures of oscillator performance</b><br/>         McNeill, J.A.;<br/>         Mixed-Signal Design, 2001. SSMSD. 2001 Southwest Symposium on<br/>         25-27 Feb. 2001 Page(s):7 - 12<br/>         Digital Object Identifier 10.1109/SSMSD.2001.914928<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF</a>(360 KB) IEEE CNF</p>  |
| <input type="checkbox"/> | <p><b>3. Design of low jitter PLL for clock generator with supply noise insensitive VCO</b><br/>         Chang-Hyeon Lee; Cornish, J.; McClellan, K.; Choma, J., Jr.;<br/>         Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on<br/>         Volume 1, 31 May-3 June 1998 Page(s):233 - 236 vol.1<br/>         Digital Object Identifier 10.1109/ISCAS.1998.704272<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF</a>(400 KB) IEEE CNF</p> |
| <input type="checkbox"/> | <p><b>4. Very short locking time PLL based on controlled gain technique</b><br/>         Fouzar, Y.; Sawan, M.; Savaria, Y.;<br/>         Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on<br/>         Volume 1, 17-20 Dec. 2000 Page(s):252 - 255 vol.1<br/>         Digital Object Identifier 10.1109/ICECS.2000.911531<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF</a>(256 KB) IEEE CNF</p>  |
| <input type="checkbox"/> | <p><b>5. VCO jitter simulation and its comparison with measurement</b><br/>         Takahashi, M.; Ogawa, K.; Kundert, K.S.;<br/>         Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia and South Pacific<br/>         18-21 Jan. 1999 Page(s):85 - 88 vol.1<br/>         Digital Object Identifier 10.1109/ASPDAC.1999.759717<br/> <a href="#">AbstractPlus</a>   Full Text: <a href="#">PDF</a>(324 KB) IEEE CNF</p>  |
| <input type="checkbox"/> | <p><b>6. A differential type CMOS phase frequency detector</b><br/>         Chang, R.C.; Lung-Chih Kuo;</p>  |

ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on  
28-30 Aug. 2000 Page(s):61 - 64  
Digital Object Identifier 10.1109/APASIC.2000.896908

[AbstractPlus](#) | Full Text: [PDF](#)(264 KB) IEEE CNF



**7. Cycle-domain simulator for phase-locked loops**

James, N.K.;  
Mixed-Signal Design, 2000. SSMSD. 2000 Southwest Symposium on  
27-29 Feb. 2000 Page(s):77 - 82  
Digital Object Identifier 10.1109/SSMSD.2000.836450

[AbstractPlus](#) | Full Text: [PDF](#)(196 KB) IEEE CNF



**8. Analysis of timing jitter in CMOS ring oscillators**

Weigandt, T.C.; Beomsup Kim; Gray, P.R.;  
Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on  
Volume 4, 30 May-2 June 1994 Page(s):27 - 30 vol.4  
Digital Object Identifier 10.1109/ISCAS.1994.409188

[AbstractPlus](#) | Full Text: [PDF](#)(324 KB) IEEE CNF



**9. Numerical modeling of PLL jitter and the impact of its non-white spectrum on the SNR of sai**

Da Dait, N.; Harteneck, M.; Sandner, C.; Wiesbauer, A.;  
Mixed-Signal Design, 2001. SSMSD. 2001 Southwest Symposium on  
25-27 Feb. 2001 Page(s):38 - 44  
Digital Object Identifier 10.1109/SSMSD.2001.914934

[AbstractPlus](#) | Full Text: [PDF](#)(496 KB) IEEE CNF



**10. A 3 V 200 MHz PLL with a low-noise VCO based on a power-efficient low-ripple DC-DC convi**

Seung-Chul Lee; Joon-Seok Lee; Sung-Ho Lee; Seung-Hoon Lee;  
VLSI and CAD, 1999. ICVC '99. 6th International Conference on  
26-27 Oct. 1999 Page(s):346 - 348  
Digital Object Identifier 10.1109/ICVC.1999.820928

[AbstractPlus](#) | Full Text: [PDF](#)(180 KB) IEEE CNF



**11. Behavioral modeling of a phase locked loop**

Phanse, A.; Shirani, R.; Rasmussen, R.; Mendel, R.; Yuan, J.S.;  
Southcon/96. Conference Record  
25-27 June 1996 Page(s):400 - 404  
Digital Object Identifier 10.1109/SOUTHC.1996.535101

[AbstractPlus](#) | Full Text: [PDF](#)(340 KB) IEEE CNF



**12. Noise response of tri-state phase frequency detector**

Sarkar, B.C.; Nandi, M.; Hati, A.; Sarkar, S.;  
Electronics Letters  
Volume 33, Issue 9, 24 April 1997 Page(s):744 - 745

[AbstractPlus](#) | Full Text: [PDF](#)(220 KB) IEE JNL



**13. A novel low jitter PLL clock generator with supply noise insensitive design**

Lin Yijing; Sheng Shimin;  
ASIC, 2001. Proceedings. 4th International Conference on  
23-25 Oct. 2001 Page(s):259 - 261  
Digital Object Identifier 10.1109/ICASIC.2001.982547

[AbstractPlus](#) | Full Text: [PDF](#)(199 KB) IEEE CNF





Welcome United States Patent and Trademark Office

☐ Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(((phase and pll and simulate and jitter)&lt;in&gt;metadata)) &lt;and&gt; (pyr &gt;= 1990 &lt;and&gt;..."

Your search matched 13 of 1203811 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

e-mail

## » Search Options

[View Session History](#)[New Search](#)

## Modify Search


☐ Check to search only within this results set

Display Format:



Citation



Citation &amp; Abstract

## » Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

## Select Article Information

- ☐ 1. **A VCO jitter performance comparison of frequency synthesizer with analog-HDL and SPICE**  
Min-Ho Kim; Jong-Wha Chong;  
TENCON 99. Proceedings of the IEEE Region 10 Conference  
Volume 2, 15-17 Sept. 1999 Page(s):1034 - 1037 vol.2  
Digital Object Identifier 10.1109/TENCON.1999.818598  
[AbstractPlus](#) | Full Text: [PDF](#)(184 KB) IEEE CNF
- ☐ 2. **A simple method for relating time- and frequency-domain measures of oscillator performance**  
McNeill, J.A.;  
Mixed-Signal Design, 2001. SSMSD. 2001 Southwest Symposium on  
25-27 Feb. 2001 Page(s):7 - 12  
Digital Object Identifier 10.1109/SSMSD.2001.914928  
[AbstractPlus](#) | Full Text: [PDF](#)(360 KB) IEEE CNF
- ☐ 3. **Design of low jitter PLL for clock generator with supply noise insensitive VCO**  
Chang-Hyeon Lee; Cornish, J.; McClellan, K.; Choma, J., Jr.;  
Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on  
Volume 1, 31 May-3 June 1998 Page(s):233 - 236 vol.1  
Digital Object Identifier 10.1109/ISCAS.1998.704272  
[AbstractPlus](#) | Full Text: [PDF](#)(400 KB) IEEE CNF
- ☐ 4. **Very short locking time PLL based on controlled gain technique**  
Fouzar, Y.; Sawan, M.; Savaria, Y.;  
Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on  
Volume 1, 17-20 Dec. 2000 Page(s):252 - 255 vol.1  
Digital Object Identifier 10.1109/ICECS.2000.911531  
[AbstractPlus](#) | Full Text: [PDF](#)(256 KB) IEEE CNF
- ☐ 5. **VCO jitter simulation and its comparison with measurement**  
Takahashi, M.; Ogawa, K.; Kundert, K.S.;  
Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia and South Pacific  
18-21 Jan. 1999 Page(s):85 - 88 vol.1  
Digital Object Identifier 10.1109/ASPDAC.1999.759717  
[AbstractPlus](#) | Full Text: [PDF](#)(324 KB) IEEE CNF
- ☐ 6. **A differential type CMOS phase frequency detector**  
Chang, R.C.; Lung-Chih Kuo;

ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on  
28-30 Aug. 2000 Page(s):61 - 64  
Digital Object Identifier 10.1109/APASIC.2000.896908  
[AbstractPlus](#) | Full Text: [PDF](#)(264 KB) IEEE CNF



**7. Cycle-domain simulator for phase-locked loops**

James, N.K.;  
Mixed-Signal Design, 2000. SSMSD. 2000 Southwest Symposium on  
27-29 Feb. 2000 Page(s):77 - 82  
Digital Object Identifier 10.1109/SSMSD.2000.836450  
[AbstractPlus](#) | Full Text: [PDF](#)(196 KB) IEEE CNF



**8. Analysis of timing jitter in CMOS ring oscillators**

Weigandt, T.C.; Beomsup Kim; Gray, P.R.;  
Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on  
Volume 4, 30 May-2 June 1994 Page(s):27 - 30 vol.4  
Digital Object Identifier 10.1109/ISCAS.1994.409188  
[AbstractPlus](#) | Full Text: [PDF](#)(324 KB) IEEE CNF



**9. Numerical modeling of PLL jitter and the impact of its non-white spectrum on the SNR of sai**

Da Dait, N.; Harteneck, M.; Sandner, C.; Wiesbauer, A.;  
Mixed-Signal Design, 2001. SSMSD. 2001 Southwest Symposium on  
25-27 Feb. 2001 Page(s):38 - 44  
Digital Object Identifier 10.1109/SSMSD.2001.914934  
[AbstractPlus](#) | Full Text: [PDF](#)(496 KB) IEEE CNF



**10. A 3 V 200 MHz PLL with a low-noise VCO based on a power-efficient low-ripple DC-DC convi**

Seung-Chul Lee; Joon-Seok Lee; Sung-Ho Lee; Seung-Hoon Lee;  
VLSI and CAD, 1999. ICVC '99. 6th International Conference on  
26-27 Oct. 1999 Page(s):346 - 348  
Digital Object Identifier 10.1109/ICVC.1999.820928  
[AbstractPlus](#) | Full Text: [PDF](#)(180 KB) IEEE CNF



**11. Behavioral modeling of a phase locked loop**

Phanse, A.; Shirani, R.; Rasmussen, R.; Mendel, R.; Yuan, J.S.;  
Southcon/96. Conference Record  
25-27 June 1996 Page(s):400 - 404  
Digital Object Identifier 10.1109/SOUTHC.1996.535101  
[AbstractPlus](#) | Full Text: [PDF](#)(340 KB) IEEE CNF



**12. Noise response of tri-state phase frequency detector**

Sarkar, B.C.; Nandi, M.; Hati, A.; Sarkar, S.;  
Electronics Letters  
Volume 33, Issue 9, 24 April 1997 Page(s):744 - 745  
[AbstractPlus](#) | Full Text: [PDF](#)(220 KB) IEE JNL



**13. A novel low jitter PLL clock generator with supply noise insensitive design**

Lin Yijing; Sheng Shimin;  
ASIC, 2001. Proceedings. 4th International Conference on  
23-25 Oct. 2001 Page(s):259 - 261  
Digital Object Identifier 10.1109/ICASIC.2001.982547  
[AbstractPlus](#) | Full Text: [PDF](#)(199 KB) IEEE CNF




[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alt](#)

Welcome United States Patent and Trademark Office

☐ Search Results[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(((phase and pll and jenkins)&lt;in&gt;metadata)) &lt;and&gt; (pyr &gt;= 1990 &lt;and&gt; pyr &lt;= ..."

Your search matched 4 of 1203811 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance in Descending order**.

e-mail

» Search Options

[View Session History](#)[New Search](#)

Modify Search

☐ Check to search only within this results set

Display Format:



Citation



Citation &amp; Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

**1. PLL phase error and power supply noise [microprocessors]**

Eckhardt, J.P.; Jenkins, K.A.;  
Electrical Performance of Electronic Packaging, 1998. IEEE 7th topical Meeting on  
26-28 Oct. 1998 Page(s):73 - 76  
Digital Object Identifier 10.1109/EPEP.1998.733753  
[AbstractPlus](#) | Full Text: [PDF](#)(312 KB) IEEE CNF

**2. Measuring jitter and phase error in microprocessor phase-locked loops**

Jenkins, K.A.; Eckhardt, J.P.;  
Design & Test of Computers, IEEE  
Volume 17, Issue 2, April-June 2000 Page(s):86 - 93  
Digital Object Identifier 10.1109/54.844337  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(116 KB) IEEE JNL

**3. Measurement of PLL phase error caused by power supply noise**

Jenkins, K.A.; Eckhardt, J.P.;  
Electronics Letters  
Volume 34, Issue 20, 1 Oct. 1998 Page(s):1907 - 1908  
[AbstractPlus](#) | Full Text: [PDF](#)(244 KB) IEE JNL

**4. A phase-locked loop clock generator for a 1 GHz microprocessor**

Boerstler, D.W.; Jenkins, K.A.;  
VLSI Circuits, 1998. Digest of Technical Papers. 1998 Symposium on  
11-13 June 1998 Page(s):212 - 213  
Digital Object Identifier 10.1109/VLSIC.1998.688088  
[AbstractPlus](#) | Full Text: [PDF](#)(244 KB) IEEE CNF

 indexed by  
[Help](#) [Contact Us](#) [Privac](#)

© Copyright 2005 IE


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alk](#)

Welcome United States Patent and Trademark Office

## Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(((decoupling and pll)&lt;in&gt;metadata))&lt;and&gt;(pyr &gt;= 1990 &lt;and&gt; pyr &lt;= 2001)"

Your search matched 10 of 1203811 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



## » Search Options

[View Session History](#)[New Search](#)

## Modify Search


☐ Check to search only within this results set

Display Format:



Citation



Citation &amp; Abstract

## » Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

## Select Article Information



## 1. Analysis of jitter due to power-supply noise in phase-locked loops

Heydari, P.; Pedram, M.;

Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000

21-24 May 2000 Page(s):443 - 446

Digital Object Identifier 10.1109/CICC.2000.852704

[AbstractPlus](#) | Full Text: [PDF](#)(376 KB) IEEE CNF

## 2. A 600 MHz CMOS PLL microprocessor clock generator with a 1.2 GHz VCO

von Kaenel, V.; Aebischer, D.; van Dongen, R.; Piguet, C.;

Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE Interna

5-7 Feb. 1998 Page(s):396 - 397, 472

Digital Object Identifier 10.1109/ISSCC.1998.672550

[AbstractPlus](#) | Full Text: [PDF](#)(1024 KB) IEEE CNF

## 3. Digitally-controlled PLL with pulse width detection mechanism for error correction

Cho, J.B.;

Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC., 1997 IEEE Intern

6-8 Feb. 1997 Page(s):334 - 335, 481

Digital Object Identifier 10.1109/ISSCC.1997.585408

[AbstractPlus](#) | Full Text: [PDF](#)(1300 KB) IEEE CNF

## 4. Low harmonics, decoupled hysteresis type current control of a multiconverter consisting of transformerless connection of VSC converters

Matakas, L., Jr.; Kaiser, W.;

Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference I IEEE

Volume 2, 5-9 Oct. 1997 Page(s):1633 - 1640 vol.2

Digital Object Identifier 10.1109/IAS.1997.629069

[AbstractPlus](#) | Full Text: [PDF](#)(616 KB) IEEE CNF

## 5. Minimum hardware solution for implementing a complete control algorithm for voltage sour

Doval-Gandoy, J.; Castro, C.; Eguizabal, L.; Penalver, C.M.;

Industrial Electronics Society, 1999. IECON '99 Proceedings. The 25th Annual Conference of the I

Volume 1, 29 Nov.-3 Dec. 1999 Page(s):490 - 495 vol.1

Digital Object Identifier 10.1109/IECON.1999.822247

[AbstractPlus](#) | Full Text: [PDF](#)(348 KB) IEEE CNF

- ☐ 6. **A fully integrated low noise RF frequency synthesizer design for mobile communication app**  
Seog-Jun Lee; Beomsup Kim; Kwiro Lee;  
VLSI Circuits, 1996. Digest of Technical Papers., 1996 Symposium on  
13-15 June 1996 Page(s):56 - 57  
Digital Object Identifier 10.1109/VLSIC.1996.507714  
[AbstractPlus](#) | Full Text: [PDF](#)(240 KB) IEEE CNF
- ☐ 7. **A fully integrated low-noise 1-GHz frequency synthesizer design for mobile communication**  
Seog-Jun Lee; Beomsup Kim; Kwiro Lee;  
Solid-State Circuits, IEEE Journal of  
Volume 32, Issue 5, May 1997 Page(s):760 - 765  
Digital Object Identifier 10.1109/4.568848  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(148 KB) IEEE JNL
- ☐ 8. **PLL synchronization for coded modulation**  
Macdonald, A.J.; Anderson, J.B.;  
Communications, 1991. ICC 91, Conference Record. IEEE International Conference on  
23-26 June 1991 Page(s):1708 - 1712 vol.3  
Digital Object Identifier 10.1109/ICC.1991.162290  
[AbstractPlus](#) | Full Text: [PDF](#)(384 KB) IEEE CNF
- ☐ 9. **Design and implementation of L1-band C/A-code GPS RF front-end chip**  
Jong-Moon Kim; Ho-Jun Song; Young-Back Kim;  
VLSI and CAD, 1999. ICVC '99. 6th International Conference on  
26-27 Oct. 1999 Page(s):372 - 375  
Digital Object Identifier 10.1109/ICVC.1999.820934  
[AbstractPlus](#) | Full Text: [PDF](#)(248 KB) IEEE CNF
- ☐ 10. **Power supply noise in future IC's: a crystal ball reading**  
Larsson, P.;  
Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999  
16-19 May 1999 Page(s):467 - 474  
Digital Object Identifier 10.1109/CICC.1999.777324  
[AbstractPlus](#) | Full Text: [PDF](#)(648 KB) IEEE CNF
- 